What is claimed is:

1. A mask-programmable read-only memory, comprising:

a first and a second address-selection lines;

a dielectric between said first and second address-selection lines;

a first memory cell, said dielectric having a first opening at said first memory cell, wherein, at the direction perpendicular to one of said first or second address-selection lines, said opening is wider than said one of address-selection lines.

2. The mask-programmable read-only memory according to claim 1, further comprising a second memory cell adjacent to said first memory cell, said dielectric having a second opening at said second memory cell, said first and second openings being portions of a single opening.

3. A non-electrically-programmable three-dimensional memory (NEP-3DM), comprising:

a substrate including transistors thereon;

at least a first and a second memory levels, said first and second memory levels being stacked on top of said substrate and said first memory level, respectively;

a plurality of inter-level connecting vias and/or contact vias, said vias connecting said memory levels with said substrate;

said memory levels comprising a plurality of memory cells, said memory cell further comprising a first address-selection line with a first width, a second address-selection line with a second width and a mask-programmable 3D-ROM layer,

4. The NEP-3DM according to claim 3, wherein said first and second memory levels share at least one address-selection line.

5. The NEP-3DM according to claim 3, wherein one dimension of said 3D-ROM layer is equal to said first width; and the other dimension of said 3D-ROM layer is equal to said second width.

6. The NEP-3DM according to claim 3, wherein said 3D-ROM layer is a natural junction between said first and second address-selection lines, said natural junction comprising portions of said first and second address-selection lines.

7. The NEP-3DM according to claim 3, wherein at least one of said address-selection lines comprises a semiconductor material doped by metallic ions.

8. The NEP-3DM according to claim 3, wherein said 3D-ROM layer is a polarized layer and/or has a polarized structure.

9. The NEP-3DM according to claim 3, wherein said memory cell is a seamless 3D-ROM cell or a quasi-seamless 3D-ROM cell.

10. The NEP-3DM according to claim 3, wherein said memory cell comprises a high-bandgap semiconductor material and/or micro-crystalline semiconductor material.

11. A non-electrically-programmable three-dimensional memory (NEP-3DM), comprising

a substrate circuit, said substrate circuit comprising a peripheral circuit, said peripheral circuit further comprising a plurality of data sense-amplifiers (S/A);

at least an NEP-3DM level stacked on said substrate circuit, said NEP-3DM level comprising at least one unit array, said unit array further comprising a plurality of NEP-3DM cells, data-bit lines and data-word lines;

a plurality of inter-level connecting vias and/or contact vias, said vias connecting said data-bit line with said data S/A.

12. The NEP-3DM according to claim 11, further comprising a first constant dc-source, and a plurality of first switches, each bit line in said unit array being connected to said first constant dc-source through a selected one of said first switches, all first switches associated with said unit array being controlled by a single first control signal.

13. The NEP-3DM according to claim 11, further comprising a second constant dc-source, and a plurality of second switches, each word line in said unit array being connected to said

second constant dc-source through a selected one of said second switches, all second switches associated with said unit array being controlled by a single second control signal.

14. The NEP-3DM according to claim 11, wherein

said data S/A further comprises a data S/A-enable (SE) signal; and

said data S/A samples the voltage on said data-bit line when said SE signal is asserted.

15. The NEP-3DM according to claim 14, wherein all data S/A in said unit array share a single data SE signal.

16. The NEP-3DM according to claim 14, further comprising a first timing bit line and an associated first timing S/A, the SE signal for said first timing S/A being connected to a constant dc-source, whereby the output from said first timing S/A eventually toggles said data SE signal and triggers the data sampling for said data-bit line.

17. The NEP-3DM according to claim 14, further comprising a second timing bit line and an associated second timing S/A, the SE signal for said second timing S/A being connected to said data SE signal, whereby the output from said second timing S/A eventually toggles said data SE signal and stops the data sampling for said data-bit line.

18. The NEP-3DM according to claim 14, further comprising a dummy-bit line, wherein

said data S/A is a differential S/A with a first input and a second input; and

said data-bit line is connected with said first input; and

said dummy-bit line is connected with said second input.

19. The NEP-3DM according to claim 11, wherein

said NEP-3DM level comprises a plurality of NEP-3DM cells, the read voltage (V_R) for said NEP-3DM cell being larger than the largest supply voltage for said NEP-3DM;

said substrate circuit further comprises a V_R-generating block.

20. The NEP-3DM according to claim 11, wherein the total number of data-bit lines in said unit array is larger than the total number of data-word lines in said unit array.